

ABSTRACT

A power source circuit includes a CMOS inversion circuit including a P-channel transistor and an N-channel transistor connected in series between a power source voltage and a reference potential, the transistors being alternately turned “on” or “off” by a PWM signal input to a gate of each transistor with an “on” period of the transistors being controlled, and being capable of outputting a D.C. voltage to a load via a stabilized capacitance. The circuit also includes a detection circuit outputting a detection signal showing a state where an intermediate node potential at a connection point of the P-channel transistor and the N-channel transistor surpasses the reference potential after undershooting to a level lower than the reference potential when the N-channel transistor is turned “on” during the “off” period of the P-channel transistor. An error amplifier is provided that obtains an error signal by comparing an output from the CMOS inversion circuit with a predetermined reference voltage value. A PWM circuit and output driver are provided that produce a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the CMOS inversion circuit, controlling the PWM signal supplied to the gate of the N-channel transistor among PWM signals supplied to the CMOS inversion circuit by the detection signal from the detection circuit, and turning “off” an “on” state of the N-channel transistor.